CS515837

GATE ARRAY APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASICs)

GENERAL SPECIFICATION FOR

CONTENTS

TABLES

ATTACHMENTS

1. SCOPE

1.1 Purpose. This document establishes the general design system, manufacturing and testing requirements for gate array Application Specific Integrated Circuit (ASIC) parts. Detailed requirements, specific characteristics of each type of ASIC, and other design-related provisions which are sensitive to the particular use of an ASIC shall be specified in the JPL-supplied individual "ST drawing" specification and design tapes for each ASIC type. The quality and reliability requirements herein provide for ASICs suitable for JPL Mission Class A and B applications.

2. APPLICABLE DOCUMENTS

2.1 Listing. This specification is based on the Level V requirements of the military specification MIL-I-38535 and Appendix B thereof, which are incorporated herein by reference. This document delineates the changes to the requirements of MIL-I-38535 which shall apply to the ASICs manufactured under this contract; these changes are noted as additions, deletions, or exceptions to requirements in the relevant paragraphs or sections of MIL-I-38535. Terms and acronyms used in this document are defined in MIL-I-38535. Other standards which delineate requirements for the ASICs are listed below and changes to these standards are noted herein. Other changes or exceptions to these documents will be defined as needed in the JPL-supplied detail specifications or in the contract.

SPECIFICATIONS

Military

MIL-I-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification for

Manufacturer

22005805	RICMOS Process Monitor, High Performance
22006409	RICMOS Layout Rules
22006410	RICMOS Electrical Rules
REL-R01	Administrative Specification for QML Electromigration Testing
REL-R03	Administrative Specification for QML Hot Carrier Testing

STANDARDS

Military

MIL-STD-883C	Test Methods and Procedures for Microelectronics (including Notices 1 through 12, except substitute for Method 1019 the test of MIL-STD-883, "Proposed Method 1019.4" dated 1/28/91 (in the contractor's possession)).

Manufacturer

SID-12404	ASIC Products Design Process Manual

2.2 General exception. If QML qualification has not yet been achieved for gate arrays, the manufacturer shall demonstrate, as a minimum, the ability to produce devices from a QML certified line and to meet the intent of the Class V requirements of MIL-M-38535.

3. REQUIREMENTS

The requirements of paragraph 3 of MIL-I-38535 apply with the following exceptions:

3.1 Wafer acceptance plan. Add the following clarifications to paragraph 3.5.1.3.3: "Tables I and II herein list the required measurements and limits for the contractor's Yield/Circuit Reliability Analysis Tool (YCRAT) monitors (equivalent to the MIL-I-38535 Technology Characterization Vehicle) and for the contractor's Process Monitor (PM) (equivalent to the MIL-I-38535 Parametric Monitor).

3.1.1 Acceptance of JPL base wafer lots. The acceptance of the JPL base wafer lots shall be contingent on evaluations of the YCRAT lots beginning fabrication closest prior to and following the beginning of fabrication of the JPL base wafer lots.

3.1.1.1 Acceptance criteria for JPL base wafer lots. The YCRATs used for acceptance of the JPL base wafer lots shall meet the following requirements:

(1) The YCRATs shall meet the evaluation criteria of Table I for the Hot Carrier and Oxide Integrity tests.

(2) The YCRAT wafers used shall be from the standard YCRAT process flow only and shall pass all of the contractor's PM acceptance criteria as specified in RICMOS III Electrical Rules Specification 22006410 at a minimum of 4 out of 5 preselected sites.

3.1.1.2 Optional procedure if yield is insufficient. In the event that the number of YCRAT wafers meeting the PM criteria is insufficient to provide the number of dice needed for reliability testing, the contractor may exercise the option of substituting wafers from either an earlier or a later (as appropriate) processed YCRAT lot for those prescribed herein. The following restrictions apply: (1)This option shall not be exercised more than once for a given lot of JPL wafers, (2) The production lot shall not be considered acceptable until the contractor has evaluated the lot of YCRATs that failed the PM criteria and can demonstrate to the satisfaction of the JPL contract technical manager that the failure mode was lot-related and not due to change(s) in the process line. If the failure was due to process line change(s), JPL may reject the production lot dice.

3.1.2 Acceptance of JPL custom wafer lots. The acceptance of JPL custom wafer lots shall be contingent on evaluations of the YCRAT lots beginning metallization closest prior to and following the beginning of customization of the JPL base wafers.

3.1.2.1 Acceptance criteria for JPL custom wafer lots. The YCRATs used for acceptance of the JPL custom wafer lots shall meet the following requirements:

(1) The YCRATs shall meet the evaluation criteria of Table I for the Electromigration test.

(2) The YCRAT wafers used shall be from the standard YCRAT process flow only and shall pass all of the contractor's PM acceptance criteria as specified in RICMOS III Electrical Rules Specification 22006410 at a minimum of 4 out of 5 preselected sites. The option described in ¶3.1.1.2 may be exercised in the event of insufficient yield.

3.1.3 Acceptance of individual JPL customized wafers. In addition to the requirements specified in the contractor's RICMOS III Electrical Rules Specification 22006410, process monitors from 5 preselected wafer sites of each JPL customized wafer shall be subjected to the Table II tests. The wafer shall be rejected if one or more of the 5 PMs fails to meet any of the parametric limits.

3.2 Part marking. Modify paragraph 3.7 as follows:

3.2.1 Serial number. A unique serial number shall be marked on each part.

3.2.2 Part identification number (PIN). Delete paragraph 3.7.2 and substitute as follows: "The part number shall be marked in accordance with the JPL detail specification. Engineering model parts shall be marked with the prefix 'EM'. The basic pattern shall be as follows:

33333-E01060FR

where:

33333 identifies the detail specification, excluding the alphabetic prefix

E identifies the JPL descriptor code for the device family

01060 is the generic or manufacturer's catalog part number (or a part thereof)

F indicates the general package style:
D = dual in-line (DIP)
F = flat pack
G = Pin-Grid Array

R identifies the level of TID testing which the lot passed (See below.)

total ionizing dose (TID) level:
M = 3 krads
D = 10 krads
N = 15 krads
S = 20 krads
P = 50 krads
Q = 75 krads
R = 100 krads
T = 150 krads
W = 200 krads
H = 1,000 krads
X, Y = unassigned: refer to detail specification

The P.I.N. in accordance with paragraphs 3.7.2 and 30.6 shall be marked on the part in addition to the JPL part number if the use of the MIL-I-38535 P.I.N. is approved by DESC."

3.3 JPL reviews of manufacturer's documentation. The manufacturer shall make available the following items to the JPL contract technical manager for review and approval prior to use with their respective JPL lots. Deviations must be approved by technical direction from the JPL contract technical manager before testing is begun.

a. Manufacturer's Quality Management (QM) plan

b. Lot traveler(s) for each part type, covering assembly, screen, and every-lot based (per Appendix B) TCI operations

c. Electrical test programs and trial data recorded from a sample device of the specified type taken over the full specified temperature range

d. Radiation test plan.

3.4 JPL QA survey or audit. JPL will perform a survey to ascertain general compliance with the Quality Management Plan prepared to satisfy the requirements of MIL-I-38535. Information regarding recent government audits, if any, shall be provided upon request.

3.5 Problem Notification. The manufacturer shall notify the JPL contract technical manager within two working days of the verification of any of the following:

a. Any catastrophic failure after initial electrical test

b. Any failures in excess of PDA, including failures which appear to result from equipment failure or operator error

c. Any QCI failure

d. Any need for re-marking serial numbers.

3.6 Data requirements.

3.6.1 Data retention. The manufacturer shall retain the lot data for a minimum of seven years.

3.6.2 Data to accompany shipments. The following data shall be included with each shipment of fully-screened flight parts:

a. a copy of the completed lot traveler(s) used for screening and TCI, showing the disposition of each serial number in the lot.

b. a copy of attributes test data, including the wafer lot acceptance test report (including SEM photos), X-ray report and films, and any applicable radiation test data

c. electrical test data for all specified tests:

1. Resolution of electrical test data shall be equal to or better than 10% of the delta limit on that parameter. In the event that the delta limits are smaller than the resolution capability of the test equipment, the limits and resolution shall be reviewed and approved by JPL.

2. If tests are labeled with test numbers, a cross-reference shall be provided to relate test numbers to descriptive test name (e.g, IIL, VOH) and pin number.

3. Electrical test data shall be provided on a magnetic medium: either IBM DOS-compatible 5-1/4" or 3-1/2" diskette with data in ASCII format or 9-track tape (800, 1600, or 6250 bpi) with data in ASCII format. In addition, one hard copy of electrical test data, formatted such that all measurements of a given parameter are displayed in a column in serial number order, shall be provided.

d. one set of data for any other special tests required by this document, the detail specification, and/or the procurement document

e. a copy of each report on any failure analyses, DPA, or engineering evaluations performed by the manufacturer

f. a copy of each waiver or Technical Direction Memorandum (TDM) altering the specified requirements.

g. a certificate of conformance with the requirements of this specification, signed by the manufacturer's authorized representative

3.7 Review of wafer lot acceptance test reports. The manufacturer shall make available at the earliest practicable time the wafer lot acceptance test report from each wafer lot from which flight parts are manufactured and

the radiation test report qualifying each flight lot to the contract technical manager for JPL review and approval. The report(s) shall be included with the data to accompany the parts at shipment. The manufacturer shall continue processing the lot: work shall not be stopped pending receipt of JPL approval.

3.8 Radiation requirements.

3.8.1 Total ionizing dose (TID). The device shall meet all functional and parametric requirements of the detail specification after exposure to a TID ≥1E5 rad (Si) at a rate ≥1 rad/sec. Note that time dependent effects (TDE) testing is not required.

3.8.2 Single event effects (SEE).

3.8.2.1 Single event upset rate (SER) (Adams' 10% worst case environment). The device SER shall not exceed 1E-9 upsets/cell/day ($\leq 2X10^{-4}$ per device/day) under the operating conditions specified in the detail specification.

3.8.2.2 Latchup. The device shall be immune to latchup at a fluence of 10^{7} ions/cm^{2} with a range >35µm and a LET of 110 MeV/mg/cm^{2}.

4. QUALITY ASSURANCE PROVISIONS

The requirements of paragraph 4 of MIL-I-38535 apply with the following exceptions:

4.1 Design requirements. Add the following to paragraph 4.2.5: "These requirements shall also satisfy as a minimum the applicable requirements of ASIC Products Design Process Manual SID-12404."

4.2 Assembly rework requirements. Modify paragraph 4.2.7.3 to indicate that no rebonding shall be allowed.

4.3 Screening.

4.3.1 Screen testing failures. Modify paragraph 4.3.1 as follows: JPL reserves the option to perform failure analysis of catastrophic failures. Screening rejects (including PIND rejects) which are not catastrophic electrical rejects shall be collected, identified as to which test was failed, and retained at the manufacturer's facility with the master set of lot data. JPL may withdraw these rejects for use as mechanical samples (e.g., for lead bending or weld schedule calibration). The manufacturer will not be required to submit these rejects to be counted by JPL QA inspectors.

4.3.2 Final electrical measurements. Clarify paragraph 4.3.7 as follows: "In the case of AC parametric vectors, at least three paths each for setup time, hold time, and propagation delay shall be measured."

4.4 Control units. Three control units shall be measured and recorded immediately before and after each set of electrical measurements of the test specimens. Each set of control unit measurements shall be checked for consistency with the last prior set of control unit measurements before proceeding with testing of the lot. In the event of significant discrepancy between two sets of readings, corrective action (maintenance or re-calibration of the test equipment) and retest of control units shall be accomplished before proceeding with testing of the lot. Note that these control units shall be used for measurements during TCI/QCI and radiation tests as well as during screening.

4.5 Getter material. No getter material shall be used inside packages.

4.6 DPA samples. The manufacturer shall make available to the JPL contract technical manager 5 samples (or 3 samples in the case of lots containing 50 parts or fewer) upon completion of the final electrical measurements of the 100% screening flow. These DPA samples may be delta rejects and/or high- and low-temperature parametric rejects. The manufacturer shall continue processing of the lot unless directed otherwise by the JPL contract technical manager. There is no lot jeopardy associated with the results of JPL's DPA unless a defect is found which is unacceptable under the terms of the contract.

4.7 JPL source inspections. JPL will perform source inspection for preseal visual (100% in accordance with method 2010 Condition A of MIL-STD-883), 100% preship external visual inspection (to method 2009 of MIL-STD-883), and preship review of the lot data books. The manufacturer shall notify JPL QA 48 hours in advance of the scheduled inspection. Adequately equipped work stations in accordance with MIL-STD-883 and MIL-STD-1686 shall be provided to the QA representatives.

4.8 Group C inspection. Add the following to paragraph 4.4.2.3: "Life test parts shall be tested for fine and gross leak in accordance with MIL-STD-883 Method 1014 after completion of the post-life test electrical measurements. There is no lot jeopardy associated with this hermeticity test."

4.9 Radiation testing. Wafer probe Aracor radiation testing shall be performed in lieu of the Group E radiation tests. The sample shall consist of 4 PMs from each of 3 wafers per lot.

4.10 Disposition of samples. Samples used for Group C life test shall be handled, packaged, and controlled in the same manner as flight parts and shipped to JPL. Any other samples used in TCI lot acceptance testing shall be retained with the master set of lot data.

4.11 Disposition of other non-flight and reject packaged parts. Any engineering prototype, engineering model, and flight parts that are rejected after packaging shall be identified as to the point at which they were rejected and made available to JPL to be used as mechanical (e.g., lead bending and weld schedule calibration) samples.

4.12 Traceability. Modify paragraph 4.2.2 as follows: Traceability shall be maintained from each serial number to the individual wafer and wafer location from which the die was selected.

5. PACKAGING

Add the following paragraphs:

5.2 Marking of container. The JPL trace number shall be marked on the initial container (i.e., unit package, e.g., tube or bag).

5.3 Packing slip and invoice. The packing slip and invoice shall include the JPL trace number associated with each line item.

6. NOTES

6.2 Terms and definitions. Modify paragraphs in MIL-I-38535 as follows:

6.2.13 Acquiring activity. Add the following: "The representative of the acquiring activity usually will be the JPL contract technical manager or contract negotiator."

6.2.14 Qualifying activity. Add the following: "If the manufacturer has not achieved QML listing, JPL will be the qualifying activity."

Add the following paragraphs:

6.2.23 Control Unit. A control unit is a part of the same device type, package, and manufacturer (but not necessarily the same lot) as the test specimens, but which is not subjected to any of the stresses that are applied to the test specimens. It is used to verify the repeatability of measurements.

6.2.24 Catastrophic Failures.

a. Opens and shorts measurable or detectable at any specified temperature or voltage

b. Any part which fails any of the subgroups 7 and 8 functional tests of MIL-I-38535 Tables III through VI

6.2.25 Contract technical manager. The contract technical manager (a member of the JPL Electronic Parts Reliability Section) shall be the principal technical interface between the manufacturer and JPL.

6.2.26 Trace number. The trace number is the number assigned by the procurement document to link a part number to a specific purchase order or order release.

6.2.27 TCI and QCI. The terms "TCI" and "QCI" are used interchangeably (consistent with MIL-I-38535) and shall refer herein to lot-based quality conformance tests in accordance with Appendix B.

EXCEPTIONS TO APPENDIX B. SPACE APPLICATION

APPENDIX B: SPACE APPLICATION

The requirements of MIL-I-38535 Appendix B apply with the following exceptions and clarifications:

B.1 Acquiring activity. Paragraphs 30.1.1 a. (prior notification of major changes) and c. (screening and TCI data) apply as requirements.

B.2 Part number. Refer to paragraph 3.2.2 herein.

B.3. Screening. Screening requirements shall be modified as follows:

B.3.1 Nondestructive bond pull. The alternate method for nondestructive bond pull (NDBP) of paragraph 40.1.a shall consist of the following:

a. Prior to bonding, the manufacturer shall perform a 100% visual inspection at high magnification of the bond pads for scratches and contamination, including oxides, per MIL-STD-883, method 2010, paragraphs 3.1.1.1 through 3.1.1.7, 3.1.2, 3.1.6.1b, and 3.1.7.

b. Prior to bonding, the manufacturer shall perform a 100% visual inspection at low magnification of the package bonding posts.

c. After bonding, a destructive bond pull test shall be performed on samples from each wire bond run. The sampling plan shall be submitted to the procuring activity for approval. The sample shall include as a minimum the first and last parts bonded in the run, and the first part bonded after any change of bonding machine setup, shift, or operator.

B.3.2 Burn-in. Modify paragraphs 40.1.d and f as follows: Two static and one dynamic burn-in shall be performed in accordance with MIL-STD-883, Method 1015. Test conditions shall be T_A=125 +3/-0°C, V_{DD}=6.5V. No accelerated burn-in is permitted. Circuits and delta limits shall be as specified in the applicable JPL detailed ("ST drawing") specification. Electrical measurements and delta calculations shall be made in accordance with Method 1015 paragraph 3.2 except that measurements shall be read and recorded for all tests required by the detailed "ST drawing" specification. In accordance with Method 1015, all measurements shall be completed within 96 hours after removal from burn-in. They shall consist (as a minimum) of Group A subgroups 1 and 7 at initial test and following each static burn-in; final measurements shall consists of Group A subgroups 1,2,3,7,8,9,10, and 11. Delta calculations shall be made following each burn-in.

B.3.2.1 Static burn-ins. Two static burn-ins of duration ≥48 hours each shall be performed prior to the dynamic burn-in. One shall be with all inputs low and the outputs tied to low through a 1KΩ resistor; the other shall be with all inputs high and the outputs tied to high through a 1KΩ resistor.

B.3.2.2 Dynamic burn-in. The dynamic burn-in shall be of duration ≥240 hours and shall be a fully functioning (full vector) burn-in. The vector set will be provided by JPL along with the individual gate array design tapes and the detailed specifications. A minimum of one output pin per device per board shall be monitored during the entire dynamic burn-in to demonstrate that the output is toggled and the circuit functioning.

B.3.3 Percent Defective Allowable (PDA). The PDA for parametric (static and functional) and delta failures cumulative across all burn-ins shall be 8% or 1 device (whichever is greater) for each inspection lot. In the event that the the first JPL lot submitted to burn-in should have a percent defective greater than or significantly less than 8%, the PDA may be adjusted (based on analysis of the cause of the defects) by mutual agreement between JPL and the Contractor. The new (negotiated) PDA shall apply to subsequent lots of JPL product. If an inspection lot exceeds the PDA but has a percent defective <15%, it may be resubmitted to burn-in one time only, with a PDA of 3% or one device (whichever is greater).

B.4 Group A test. Modify paragraph 40.2 item a as follows: Group A tests shall be imposed as a 100% screen regardless of lot size.

B.5 Life test. Modify paragraph 40.2 item c. for Group C to change required life test duration from 1000 hours to 2000 hours. Test conditions shall be T_A=125 +3/-0°C, V_{DD}=6.0V. Actual devices shall be tested, with an accept criterion of 22(0) for lots ≥48 parts. Post-life test electrical measurements and delta calculations shall be recorded as specified above (paragraph B.3.2) for final electrical measurements in screening.

ATTACHMENT 1. SPECIFICATION FOR BREAKDOWN VOLTAGE TESTING

Testing shall be performed by wafer probe at room temperature.

The wafer lot used for the TCV wearout testing shall undergo Wafer Lot Acceptance (QA Operating Procedure QA-75) and shall meet PM critical parameter test limits (documented in RICMOS III Electrical Rules Specification, 22006410.

Testing shall be performed on 3082-cell transistor arrays ("arrays") from the Parallel Transistor Array Defect Test Structure (PTADTS) of the contractor's YCRAT, part number 22005310.

Arrays shall be biased in accumulation, i.e., n-type arrays shall be biased with the transistor gates negative relative to the source, drain and substrate; p-type arrays shall be biased with the transistor gates positive relative to the source, drain, and well.

The bias voltage on each array shall be increased in steps until the array fails. The gate current shall be measured at each step. Current in excess of 10 A/cm^2 shall constitute a failure of the array.

The breakdown voltage shall be recorded for each array. Histograms and cumulative distributions shall be prepared showing, for n-type and p-type arrays separately, the number of arrays as a function of the breakdown voltage.

ATTACHMENT 2. SPECIFICATION FOR ELECTROMIGRATION TESTING

The contractor's Administrative Specification REL-R01 shall be modified as follows:

Testing shall be performed on 10 structures of each type from each YCRAT lot.

Testing of straight stripes shall be replaced by testing of Metal 1 and Metal 2 meander structures from the Topographical Reliability Test Structure (TRTS). Metal 1 and Metal 2 meanders shall be selected from different dice.

During testing of the meander structures, the resistance between the meander and the interdigitated extrusion monitor shall be measured regularly. An extrusion failure shall consist of a resistance measurement <1MΩ.

Stress conditions and failure criteria shall be in accordance with Table I herein.

Table I. Reliability Monitors: YCRAT(Contractor-Designed)

PARAMETER	STRUCTURE	STRESS CONDITION	EVALUATION	
			MEDIAN TIME TO FAIL (MIN)	Δ LI CRIT
1. Hot Carrier [a]	1.2µm gate length N-channel transistors	T=-55°C, V_{DS}=6V, V_{GS}=3V	550 minutes	-10%
2. Oxide integrity (TDDB) [b]	n- and p-type large (3082- element) transistor arrays	Ramp voltage @ rate of 1V/sec, with step sizes of 0.25V/0.25 sec.	N/A	>5 o p-ty volt
3. Electro-migration [c]		@ T_A=250°C		
	n^+ contact string	15 mA	58 hours	+10%
	p^+ contact string	12 mA	150 hours	+10%
	via string	24 mA	140 hours	+20%
	metal 1 meander	15 mA	100 hours	+10% or e
	metal 2 meander	40 mA	100 hours	+10% extr

Notes:
(a) Hot carrier testing shall be performed on 8 dice from each of 3 wafers per YCRAT lot. performed in accordance with the contractor's specification REL-R03, as modified by this t
(b) Oxide integrity testing shall be performed on a minimum of 200 each of n-type and p-ty transistor arrays from each YCRAT lot. These quantities shall exclude those with an initi @ 2.0V. Breakdown voltage tests shall be performed in accordance with Attachment 1.
(c) Electromigration testing shall be performed on 10 dice per YCRAT lot in accordance wit specification REL-R01 as modified by this table and Attachment 2.

Table II. Process Monitor (Contractor Designed)
Five-Sites/Wafer Room Temperature Measurements

Wafer Number: _____ Date: _

Parameter	Device	Lower Limit	Upper Limit	Unit	No. Good	Mean	ST
1.1 Gate Threshold Voltage	nMOS W/L=10/1.2µm	0.90	1.50	V			
1.2 Gate Threshold Voltage	pMOS W/L=10/1.2µm	-1.15	-0.55	V			
1.3 Drive Current (Ion)	nMOS W/L=10/1.2µm	1.30	1.85	mA			
1.4 Drive Current (Ion)	pMOS W/L=10/1.2µm	-1.35	-0.70	mA			
1.5 Field Threshold Voltage	nFET W/L=100/2.6µm	15.00		V			
1.6 Field Threshold Voltage	pFET W/L=100/2.6µm	-15.00		V			
1.7 Breakdown Voltage	nMOS W/L=10/1.2µm	8.00		V			
1.8 Breakdown Voltage	pMOS W/L=10/1.2µm	-8.00		V			
1.9 Breakdown Voltage	nMOS W/L=300/1.2µm	8.00		V			
1.10 Breakdown Voltage	pMOS W/L=300/1.2µm	-8.00		V			
1.11 Breakdown Voltage	nFET W/L=100/2.6µm	8.00		V			
1.12 Breakdown Voltage	pFET W/L=100/2.6µm	-8.00		V			
1.13 Kprime (µCo/2)	nMOS W/L=100/10µm	44.00	88.00	$\mu A/V^2$			
1.14 Kprime (µCo/2)	pMOS W/L=100/10µm	13.00	27.00	$\mu A/V^2$			
1.15 Transconductance (MAX)	nMOS W/L=10/1.2µm	21.00	63.00	µmho			
1.16 Linewidth (meas.-drawn)	First Metal	-0.40		µm			
1.17 Linewidth (meas.-drawn)	Second Metal	-0.60		µm			
1.18 Schottky Diode	Vforward	0.20	0.60	V			
1.19 Schottky Diode	Reverse Breakdown	8.00		V			
1.20 Schottky Diode	Reverse Leakage	-	100.00	nA			
1.21 Vertical PNP Gain Beta	pMOS W/L=50/1.2µm	6.00	12.50	-			
1.22 Delay Line (50 stages)	W/L=10/1.2µm	24.50	50.20	ns			
1.23 Sheet Resistance	N+	56.00	80.00	Ω/□			
1.24 Sheet Resistance	P+	83.00	127.00	Ω/□			
1.25 Sheet Resistance	Poly	20.00	60.00	Ω/□			
1.26 Sheet Resistance	N-TUB	525.00	875.00	Ω/□			
1.27 Sheet Resistance	M1	0.04	0.12	Ω/□			
1.28 Sheet Resistance	M2	0.02	0.06	Ω/□			
1.29 Contact Resistance	M1/N+ (1.5x1.5μm^2)	8.00	32.00	Ω			
1.30 Contact Resistance	M1/P+ (1.5x1.5μm^2)	15.00	55.00	Ω			
1.31 Contact Resistance	M1/Poly (1.5x1.5μm^2)	5.50	30.00	Ω			

1.32 Via Resistance	M2/M1 ($2.0x2.0\mu m^2$)	0.03	0.20	Ω

Filename: CS515837.B
Directory: H:\USERS\514\SPECS\ACT-GENL
Template: F:\USERS\JSANSONE\MSOFFICE\WINWORD\TEMPLATE\NORMAL.DOT
Title:
Subject:
Author: Jennifer Sansone
Keywords:
Comments:
Creation Date: 08/10/95 2:21 PM
Revision Number: 1
Last Saved On:
Last Saved By:
Total Editing Time: 1 Minute
Last Printed On: 08/10/95 2:28 PM
As of Last Complete Printing
Number of Pages: 24
Number of Words: 5,011 (approx.)
Number of Characters: 28,563 (approx.)